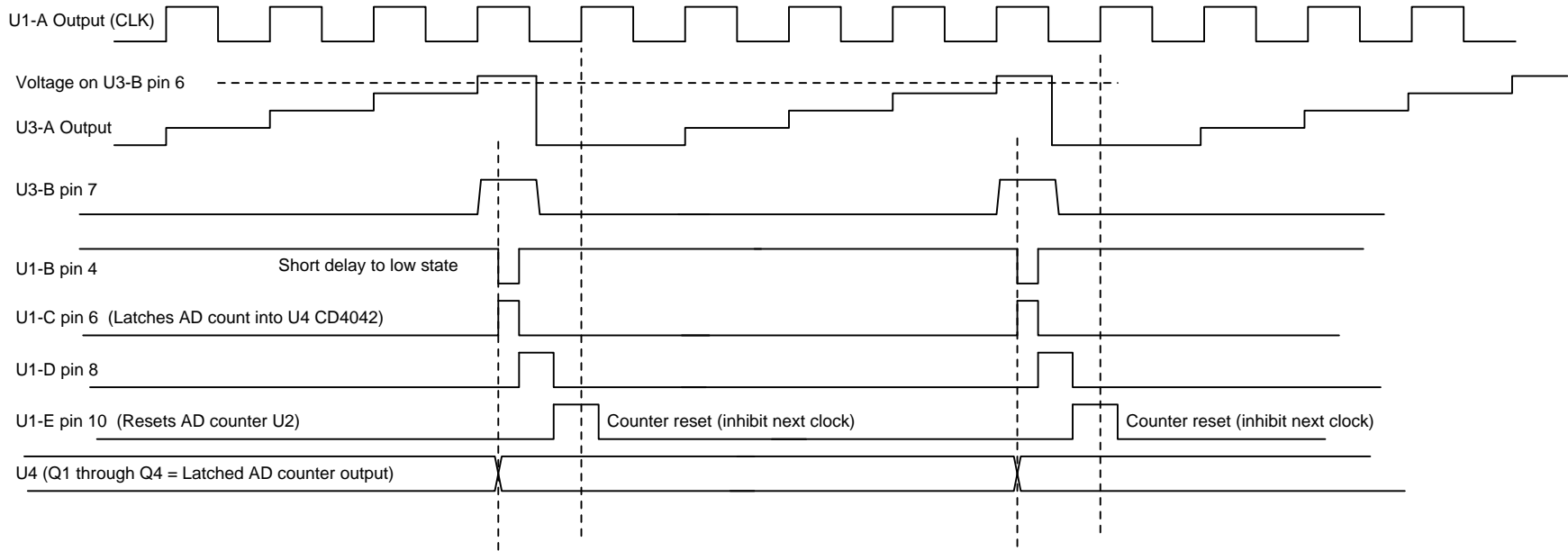


A to D Converter Logic Timing Diagram (AD count greater than 0)



A to D Converter Logic Timing Diagram (AD count equal 0)

