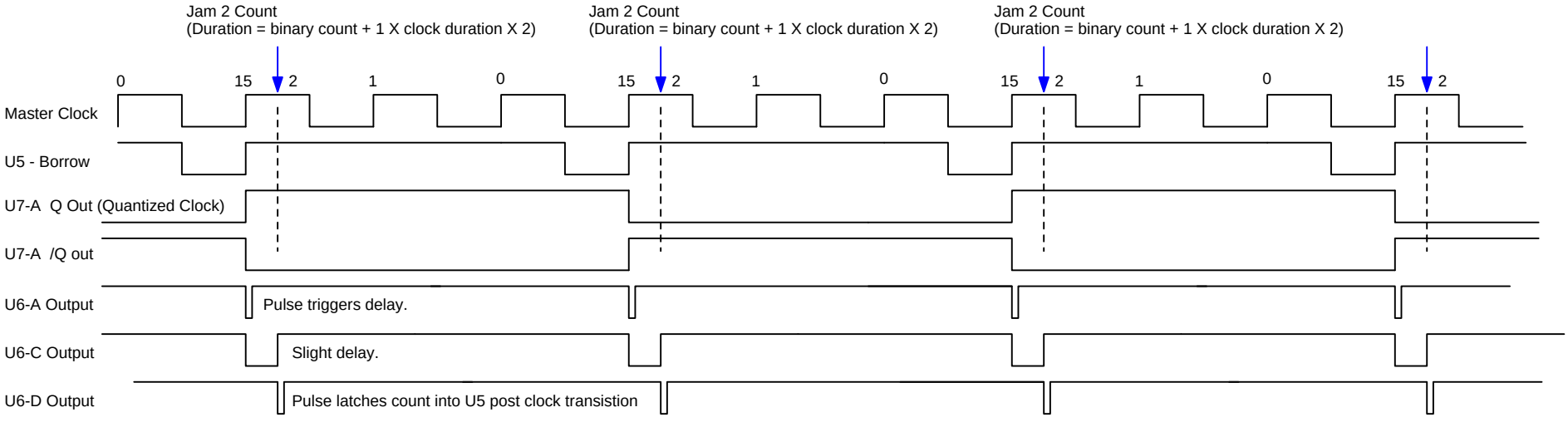
Time Quantization Logic Timing Diagram (Count above binary 0)

Time step set to binary 2 (+1 = 3 clocks)
for illustration.

Notice that the "Quantized clock" has both positive and negative phases timed.



Time Quantization Logic Timing Diagram (Count equal binary 0)

Notice that the "Quantized clock" has both positive and negative phases timed.

Time step set to binary 0 (+1 = 1 clock)
for illustration.