Sustain With Gated Operation

0
Ready State

1

2

Threshold voltage used for sustain timing. When set to be near or at the previous threshold voltage this segment may be spuriously skipped over.

3

4

0
Ready State

< 500uS

Sustain would normally end here in triggered mode but it is extended by the presence of the Gate in modes 1 and 2.

In Gate mode 1 if the gate is removed before the sustain segment is completed the module clocks to the next segment immediately.

S1 set to 4 segment envelope causes return to ready state at the start of segment 5.

Gate pulse

U3-B Pin 3

U3-C Pin 6 — Reset U6 to Ready State

U3-E Pin 10 — Jam count "0001" into U6

U5-A Pin 1
U5-C Pin 6

U5-A Pin 2

U5-B Pin 4

End of ramp detect disabled.

9V

U7-D Pin 14

U5-D Pin 8

U9-F pin 12 — End of gate clock

U6 Pin 14

Raw Ramp (RR)

Threshold Voltage (THV)

In Gate mode 2 the envelope would end here (on Gate release) and return to Ready state.